What is claimed is:

1. An array substrate for use in an IPS-LCD device, comprising:

a plurality of double-layered gate lines on a substrate, wherein the double-layered gate lines are comprised of first and second layers that overlap each other;

a plurality of data lines over the substrate, wherein each data line is perpendicular to each double-layered gate line, and wherein each pair of double-layered gate and data lines defines a pixel area;

a double-layered common line on the substrate, wherein the double-layered common line is parallel with and spaced apart from the double-layered gate line, and wherein the double-layered common line is comprised of first and second layers that overlap each other;

a plurality of protrusions extending from first layer of the double-layered gate lines, wherein each protrusion has a hole in a central portion thereof;

a plurality of common electrodes extending from the second layer of the double-layered common line and parallel with the data line;

a common-connecting line perpendicular to and connecting the common electrodes with each other;

a plurality of pixel electrodes spaced apart from and parallel with the said common electrodes, wherein each pixel electrode is located between a pair of common electrodes and corresponds to at least one common electrode;

first and second pixel-connecting lines parallel with the double-layered common line and respectively connecting the pixel electrodes with each other at respective first and second ends of the pixel electrodes, wherein the second pixel-connecting line overlaps a portion of the double-layered common line to form a storage

capacitor; and

a switching element electrically located in one corner of the pixel area and connected with the double-layered gate and data lines, the switching element contacting the first pixel-connecting line and supplying voltage to the said pixel electrodes.

2. The array substrate according to claim 1, further comprising: a gate insulation layer covering the substrate and the double-layered gate lines and the double-layered common lines.

3. The array substrate according to claim 1, further comprising: a passivation layer formed over the swiching element and having a drain contact hole and an etching hole.

4. The array substrate according to claim 3, wherein the etching hole is formed over a portion of each protrusion.

5. The array substrate accoding to claim 3, wherein the switching element includes a source electrode that extends from the data line; a double-layered gate electrode that extends from the double-layered gate line; a drain electrode that contacts the first pixel-connecting line through the drain contact hole; an active layer over the double-layered gate electrode; and ohmic contact layer interposed between the active layer and the source and drain electrodes.

6. The array substrate according to claim 5, wherein the source and drain electrodes and the data lines are made of the metallic material selected from a group consisting of chromium (Cr), aluminum (Al), aluminum alloy (Al alloy), molybdenum (Mo), tantalum (Ta), tungsten (W), and antimony (Sb).

7. The array substrate according to claim 1, wherein the double-layered common line is made of the same material of the double-layered gate lines and formed in the same layer of the double-layered gate lines.

8. The array substrate according to claim 1, wherein the protrusions extended from the first layer of the double-layered common line are located on both sides of the storage capacitor.

9. The array substrate according to claim 1, wherein each protrusion has a quadrilateral shape.

10. The array substrate according to claim 1, wherein each protrusion has a quadrilateral-shaped hole in a central portion of the protrusion.

11. The array substrate according to claim 1, wherein the first layers of the double-layered gate and common lines include aluminium (Al).

12. The array substrate according to claim 1, wherein the second layers of the double-layered gate and common lines are made of Molybdenum (Mo)

13. The array substrate according to claim 1, wherein the second layers of the double-layered gate and common lines are made of Chrome (Cr).

14. A method of fabricating an array substrate for use in an IPS-LCD device, comprising:

depositing a first metallic material on a substrate;

patterning the first metallic material to form a first gate electrode, a first gate line, a first common line, and a plurality of protrusions, wherein each protrusion has a hole in a central portion thereof and extends from the first common line, and wherein the first gate electrode extends from the first gate line;

depositing a second metallic material on the substrate and on the patterned first metallic material;

patterning the second metallic material to form a second gate electrode, second gate line, second common line, a common-connecting line, and a plurality of common electrodes, wherein the first and second gate electrodes overlap each other to form a double-layered gate electrode, wherein the first and second common lines overlap each other to form a double-layered common line, and wherein the first and second gate lines overlap each other to form a double-layered gate line;

forming a gate insulation layer on the substrate and on the patterned second metallic material;

forming an active layer and an ohmic contact layer sequentially on the gate insulation layer and over the double-layered gate electrodes;

depositing a third metallic material on the ohmic contact layer and on the gate

insulation layer;

forming a data line, a source electrode, and a drain electrode by patterning the third metallic material, wherein the source and drain electrodes are over the double-layered gate electrodes, and wherein the data line is perpendicular to both the double-layered gate lines and double-layered common lines;

forming a passivation layer on the patterned third metallic layer and on the gate insulation layer, wherein the passivation layer has a drain contact hole to the drain electrode, and an etching hole over each protrusion;

depositing a transparent conductive material on the passivation layer having the drain contact hole and the etching hole; and

forming a plurality of pixel electrodes and first and second connecting lines.

15. A method of fabricating an array substrate according to calim 14, further comprising: forming a channel region by patterning a portion of the ohmic contact layer between the source and drain electrodes.

16. A method of fabricating an array substrate according to claim 14, wherein each pair of double-layered gate lines and data lines defines a pixel area.

17. A method of fabricating an array substrate according to claim 14, wherein the double-layered common line is parallel with and spaced apart from the double-layered gate line.

18. A method of fabricating an array substrate according to claim 14, wherein a plurality of the common electrodes are parallel with the data line.

19. A method of fabricating an array substrate according to claim 14, wherein the common-connecting line is perpendicular to and connects the plural common electrodes with each other.

20. A method of fabricating an array substrate according to claim 14, wherein a plurality of the pixel electrodes are spaced apart from and parallel with the said common electrodes.

21. A method of fabricating an array substrate according to claim 14, wherein each pixel electrode is located between the pair of common electrodes and corresponds to each common electrode.

22. A method of fabricating an array substrate according to claim 14, wherein the first and second pixel-connecting lines are parallel with the double-layered common line and respectively connect the pixel electrodes to each other at respective first and second ends of the pixel electrodes.

23. A method of fabricating an array substrate according to claim 14, wherein the second pixel-connecting line overlaps a portion of the double-layered common line to form a storage capacitor.

24. The array substrate according to claim 23, wherein the protrusions extended from the first common line are located on both sides of the storage capacitor.

25. A method of fabricating an array substrate according to claim 14, wherein the double-layered gate electrode, the active layer, the ohmic contact layer, the source electrode and the drain electrode comprise a thin film transistor that is located near the crossing of a double-layer gate line and data line.

26. A method of fabricating an array substrate according to claim 14, wherein the third metallic material is selected from a group consisting of chromium (Cr), aluminum (Al), aluminum alloy (Al alloy), molybdenum (Mo), tantalum (Ta), tungsten (W), and antimony (Sb).

27. A method of fabricating an array substrate according to claim 14, wherein the double-layered common line is made of the same material as the double-layered gate lines and formed in the same layer as the double-layered gate lines.

28. A method of fabricating an array substrate according to claim 14, wherein each protrusion has a quadrilateral shape.

29. A method of fabricating an array substrate according to claim 14, wherein each protrusion has a quadrilateral-shaped hole in a central portion thereof.

30. A method of fabricating an array substrate according to claim 14, wherein the first metallic material includes aluminium (Al).

31. A method of fabricating an array substrate according to claim 14, wherein the second metallic material is selected from a group consisting of molybdenum (Mo), chrome (Cr) and tungsten (W).

32. A liquid crystal display device, comprising:

first and second substrates;

a plurality of data lines on the first substrate;

a plurality of gate lines on the first substrate perpendicular to the data lines;

wherein a pixel region is defined by the intersection of one of the gate lines and one of the data lines;

a common line in the pixel region parallel to the gate lines;

a plurality of common electrodes in the pixel region parallel to the data lines and extending from the common line;

a thin film transistor in the pixel region near the intersection of the one gate line and the one data line, the thin film transisor having a source electrode, a gate electrode and a drain electrode;

a protrusion extending from the common line; and

a liquid crystal layer interposed between the first and second substrates.

33. The liquid crystal display device of claim 32, wherein at least one of said gate lines comprises a first gate line layer and a second gate line layer.

34. The liquid crystal display device of claim 32, wherein the common line comprises a first common line layer and a second common line layer.

35. The liquid crystal display device of claim 34, wherein the protrusion extends from the first common line layer.

36. The liquid crystal display device of claim 32, wherein the protrusion is a quadrilateral shape.

37. The liquid crystal display device of claim 36, wherein the protrusion is a square shape.

38. The liquid crystal display device of claim 32, wherein the protrusion includes an aperture in a central portion thereof.

39. The liquid crystal display device of claim 32, further comprising an aperture in the protrusion.

40. The liquid crystal display device of claim 35, wherein the second common line layer is on the first common line layer.

41. The liquid crystal display device of claim 33, wherein the first gate line layer comprises aluminum.

42. The liquid crystal display device of claim 33, wherein the second gate line layer comprises a metal selected from a group consisting of molybdenum (Mo), choromium (Cr) and tungsten (W).

43. The liquid crystal display device of claim 34, wherein the first common line layer comprises aluminum.

44. The liquid crystal display device of claim 34, wherein the second common line layer comprises a metal selected from a group consisting of molybdenum (Mo), choromium (Cr) and tungsten (W).

45. The liquid crystal display device of claim 32, further comprising an etching hole over a portion of the protrusion.

46. The liquid crystal display device of claim 38, further comprising an etching hole over the aperture.